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WHITE PAPER

# AMS Emulation Comes to the Rescue with Rapid, Pre-Silicon DDR Verification


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## Abstract

State-of-the-art SoCs incorporate a plethora of analog mixed-signal (AMS) components, such as serializers/de-serializers (SERDES), power conditioners, converters, filters, and high-speed double data rate (DDR) memory (Figure 1). Many of these components require firmware for equalization, calibration, tuning, and configuration. The designs are complex and a challenge for hardware verification. Validation of them working under software control, pre-silicon, has been largely impossible. This creates a problem for both commercial firms and governmental organizations.

This white paper presents Synopsys AMS Emulation, a novel and unique solution whereby hardware-based emulation is enhanced to overcome the many limitations of current accelerated simulation technology. Digital-logic-only emulators lack support for floating-point valued signals, analog math operations, timing of intermixed analog and digital logic controls, analog output, and other requirements of AMS design verification. AMS Emulation provides this support and delivers much faster performance than software-based simulation.

DDR5 calibration serves as a demonstration of this new capability, since this interface is very common yet challenging to verify due to its timing complexity, the need for firmware support when run at high speeds, and the criticality of verifying transport delay. Digital-only emulators lack support for transport delay, the time between when a memory controller accesses a specific RAM memory location and when the data becomes available. This delay varies, which is a challenge for emulators with fixed clock cycles (Figure 2). AMS Emulation provides the support required.

In addition to support of AMS components in conjunction with digital processing and software execution, AMS Emulation provides nearly 100x verification performance increase over software-based simulation, as proven using several industrial designs. Based on this success, AMS emulation is today being used by several leading-edge semiconductor companies.



This first-in-the-industry enabling of AMS emulation that provides pre-silicon system software validation was made possible through funding of the Posh Open Source Hardware (POSH) Program by the Defense Advanced Research Programs Agency (DARPA).

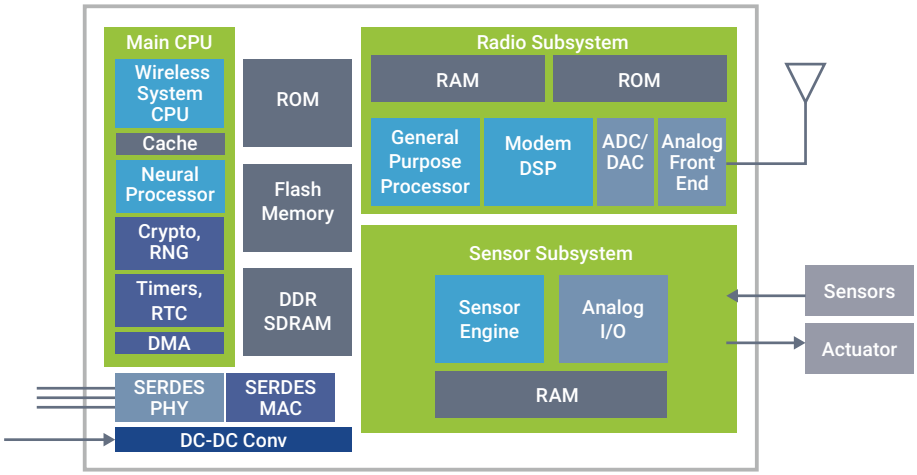


Figure 1: Modern-day SoC with many AMS components

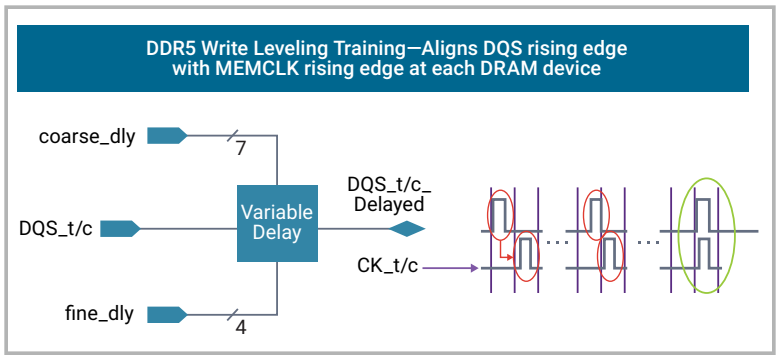


Figure 2: DDR transport delay enabled in emulation

## AMS Emulation: A New Standard in AMS Verification

Modern-day SoC designs predominately incorporate digital-based processing, usually controlled by software or firmware. Often, the system inputs and outputs are analog in nature, such as sensors or audio signals, or are assisted by analog circuitry to compensate for real-world conditions that attenuate or inject unwanted noise. In addition, systems use analog components to ensure a satisfactory voltage source and clock frequency, and to sense environmental factors, such as temperature. Software running on the internal processor ensures that the voltage and frequency are stable, and that the system is ready to communicate with its memory and external connections.

Depending on the application, these connections could be AMS inputs, such as sensors, antennas, audio/video, network, and other communications peripherals. AMS outputs controlled by the SoC may be actuators, transducers, audio/video, network, and other communications peripherals. These peripherals may require equalization, gain control, filtering, encoding/decoding, analog-to-digital or digital-to-analog conversion, serial-to-parallel or parallel-to-serial conversion, and clocking. Sensors include temperature, voltage, acceleration, magnetic field, gyroscopes, and biometrics. Typically, there are many AMS circuits internal to, and on the periphery of, the SoC that the chip reacts to and/or controls, some of which are operated by software drivers.

Verification of the entire system, inclusive of its digital, analog, and software components, is a well-known industry challenge. Many verification advances, specifically hardware-based emulation, which can rapidly simulate operation of a large system running software, currently do not support the analog portions. Instead, analog designs are verified on much slower software-based circuit simulators in SPICE or abstracted model representations. The solution is Synopsys AMS Emulation technology, a novel approach for pre-silicon verification of AMS systems requiring calibration firmware, developed from a collaboration with DARPA through its POSH program. It results in a unique and first-of-its-kind emulation platform, including digital and analog hardware and providing pre-silicon system-level verification at a nearly 100x improvement in performance over AMS software-based simulation.

## Software: Critical to System Validation

The continual demand for faster computation requires data to be quickly available from memory. This requirement, plus a similar desire for data to be rapidly transferred between systems and their external interfaces, led to the invention of high-speed peripherals, many of which are enabled through complex SERDES components that account for mismatched impedances and other real-world phenomena. Fast memory interfaces operate similarly by embedding the clock signal in the data stream to convert parallel signal paths to/from serial ones. Different applications and operating environments (such as board layout) are accommodated through programming of control registers. For example, for SERDES-based peripherals, the serial output swing can be programmatically increased to reach a longer distance or decreased to reduce power. Similarly, the amount of output de-emphasis can be adjusted based on the link length.

Adapting the hardware to changing environmental conditions is difficult to achieve using fixed parameter values. Instead, the hardware is more agile and extensible if the parameters can be set dynamically, based on real-world phenomena such as PCB impedance. Calibration software performs this role, continuously changing different parameter values and testing their effect on circuit operation to find the optimal settings. Making the SERDES hardware programmable means that it can be tailored to meet the specific needs of a given application [1]. However, hardware configurability must be verified along with proper circuit operation. Therefore, software, such as drivers that control the hardware, must be part of system validation.

## Software Programmability Enables Rapid DDR Calibration

DDR memories share the same need for configurability during system bring-up that cannot be set statically at design time. After power-up and initialization, there are several parameters in a DDR memory that must be calibrated, including [2]:

- Write leveling
- Data strobe (DQS) gating
- Read data eye
- Write data eye

Write leveling adjusts the timing of the write DQS signals relative to the DDR clock. DQS gating determines when the read DQS signal is valid. Read data eye aligns the read DQS signal to the center of the valid read data. Write data eye aligns the write DQS signal to the center of the valid write data.

An example of a DDR memory channel is displayed in Figure 3.

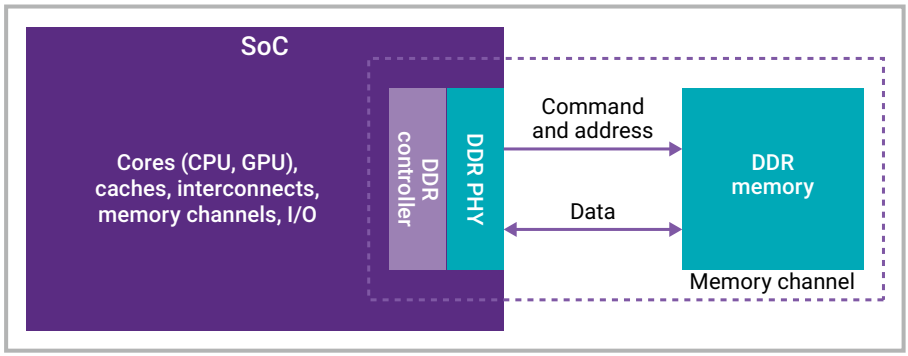


Figure 3: Memory channel block diagram

After DDR calibration, ensuring reliable and robust links in the memory channel requires the memory interface to be trained [3]. According to the JEDEC Solid State Technology Association specifications, full training is an iterative process involving changing a parameter, testing for correct memory access, and then repeating that process. A sense of the training complexity is shown in Figure 4. The sequence includes chip select/command address (CS/CA) training, read training, duty cycle adjustment (DCA) training, distributed feedback equalization (DFE) training, write training, and physical layer (PHY) training.

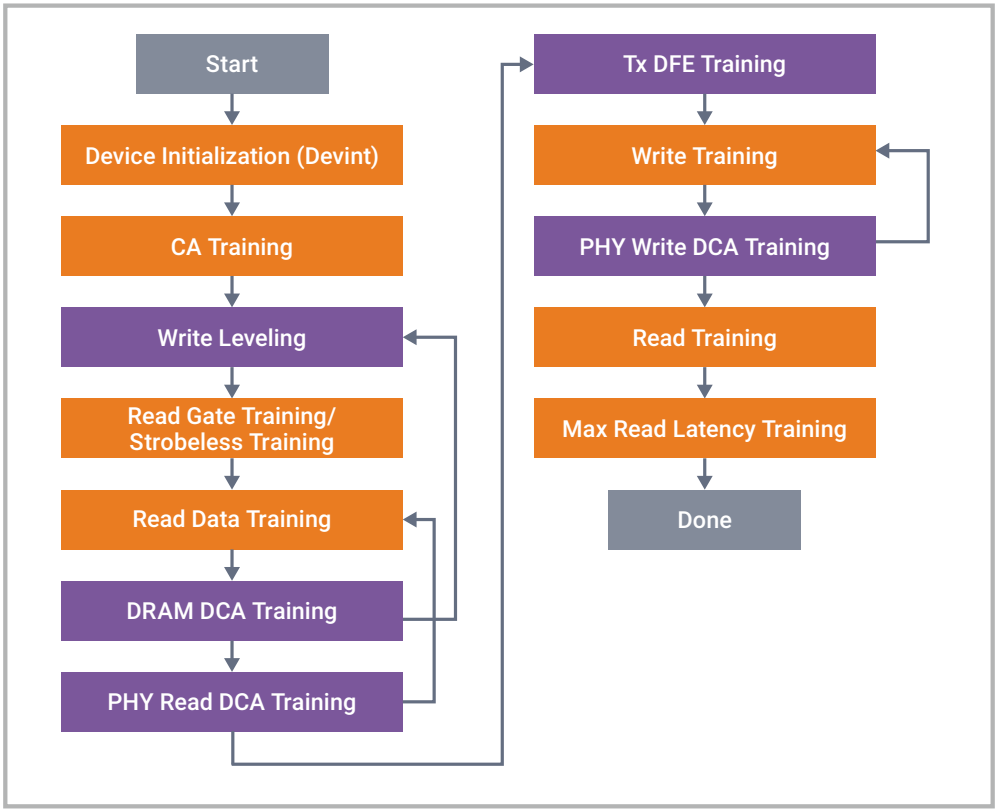


Figure 4: DDR training

SERDES programming, DDR training, filter calibration, and equalization can be accomplished through hardware; for example, using finite state machines. However, this approach has many disadvantages, such as the inability to accommodate field upgrades to fix bugs or implement new standards. Using firmware is a better approach since it can be updated in the field. Efficient pre-silicon hardware-software co-verification of hardware and firmware presents challenges, and the following sections explain how Synopsys AMS Emulation technology provides a solution.

## DDR PHY Modeling with Real Number Models

A primary problem faced by AMS SoC verification that include components such as DDR memory is the traditionally distinct methods used in the analog and digital domains. Analog circuits operate in continuous time while digital signals only change at discrete intervals. The verification tools and techniques applied differ, since the circuit simulation behavior of each domain is different. As the amount of digital content per SoC exploded, many methods were employed to maintain digital design verification performance. The ultimate digital technique is automatically programming custom hardware to emulate those designs and thereby executing the logic at speeds typically in tens of megahertz (emulation). On the other hand, simulators such as SPICE that mimic the behavior of analog circuitry run multiple orders of magnitude slower. Thus, although SoC verification performance must scale as fast or faster as does design size and complexity, the analog/AMS portions have not been capable of meeting this requirement.

A solution to this dilemma is to describe the analog circuit behavior in such a way that the much faster digital verification techniques can be utilized. This is where Real Number Models (RNM) provide their benefit. RNMs allow for the representation of floating-point real numbers and a signal flow description of analog circuit behavior that can be evaluated in discrete time. For example, the 2017 Panhellenic Conference on Electronics and Telecommunications paper entitled Real Number Modeling of a Flash ADC Using SystemVerilog compares the verification performance of an RNM equivalent of a three-bit analog-to-digital converter (ADC) against its analog-based representation. The paper concludes: “The experiments pointed out the high simulation efficiency of [RNM] modeling, along with acceptable accuracy, in comparison with the rest of the mixed-signal or analog modeling methods. Considering that a flash ADC can be used in numerous applications like wideband radio receivers, electronics test equipment and many others, the gain in simulation speed can be significant” [5].

## Emulation with Real Number Models

The next challenge is rapid simulation of the DDR RNM model with firmware running on a processor. Digital simulators were enhanced to support RNMs and co-simulate them with digital content. This approach provides about a 10X performance increase over analog simulation but remains too slow for running firmware in conjunction with the models.

Emulation is hardware-assisted simulation. Dedicated hardware, typically based on FPGA technology, provides one or more orders of magnitude performance increase over software simulators such as Synopsys VCS. An example of such a system is the Synopsys ZeBu emulator shown in Figure 5.


Figure 5: Synopsys ZeBu Server 4 emulation system

Emulation is very good at handling digital circuits. Due to the high speed of digital circuits, they can execute processor cycles fast enough to run software programs up to 10Mhz [6]. This capability enables software and hardware to be verified together pre-silicon. However, to support AMS RMS, emulators must be able to operate with non-emulatable syntax, such as floating-point signal values, user- defined functions, nettypes, and delay statements. RNM support must also include accurately representing the range of voltages and signal chain functions present with analog circuits using hardware that at its core is digital. Analog operations must execute alongside Boolean digital logic. Additionally, timing of the analog and digital portions of the design must be synchronized.

A further complication arises specifically for DDR emulation regarding write leveling calibration. Transport delay refers to the variable timing of the DQS (data quality strobe) signal rising edge with respect to the memory clock rising edge (see Figure 2). This concept is difficult to emulate with static timing programmed into FPGAs because the delay is dynamic, with the firmware calculating new coarse/fine register values based on the samples received during training. It is a challenge to support timing delay that varies if all other timing delays are fixed. The RNM expression the emulator must support is displayed in Figure 6.

```
`timescale 1ns/100fs

real zerodelay = 0.111, real stepsize = 0.0023, real pvtscale = 1;

reg [6:0] coarse_dly, reg [3:0] fine_dly;

always @* begin
  dly_out_var <= #(zerodelay + ((((dly_selcoarse_total*8)+dly_selfine_total) * stepsize)*pvtscale)) dly_in_int;
end
```

Figure 6: Expression of DDR transport delay

These challenges have been overcome with the AMS Emulation capability developed for the ZeBu emulation platform. AMS RNMs are parsed and assigned to internal FPGAs and DSPs that are globally clocked to enable concurrent simulation of analog and digital circuit behavior. This feature allows firmware to be executed on a digital processor to perform DDR memory calibration. Figure 7 illustrates how the behavior of the analog portion is extracted, analyzed, converted to RNM, combined with the digital parts, and run on the emulator using software-based stimulus.

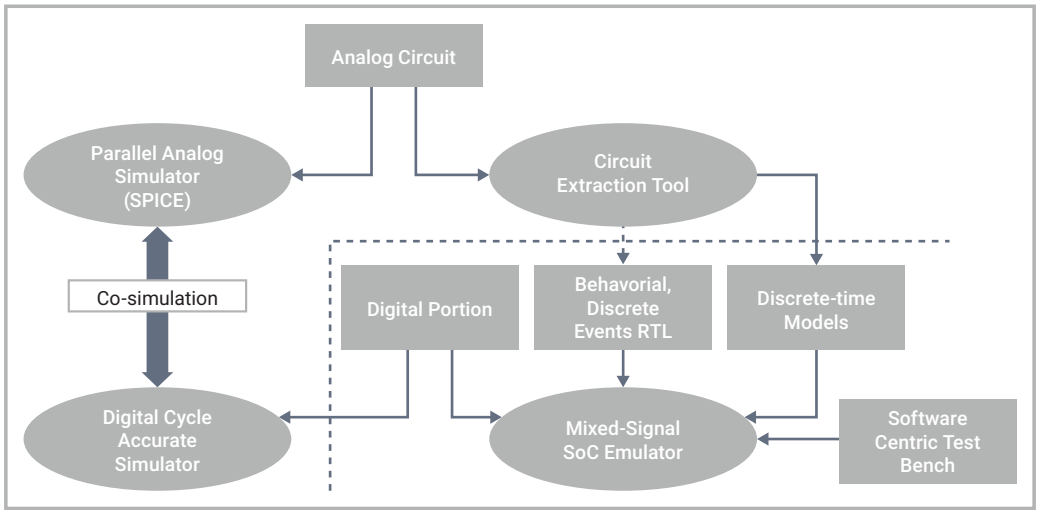


Figure 7: Adopting AMS content to emulation

## Results: Rapid Pre-Silicon Validation of the DDR PHY Calibration Sequence

A commercial DDR5 PHY from a leading semiconductor design firm was previously unable to be verified pre-silicon. The PHY was expressed as a real number model, but it could not be checked in the context of its calibration software within a feasible time using software simulation. The RNM was then executed with its firmware on a ZeBu emulator using the AMS Emulation feature.

Figures 8 and 9, respectively, show the time required for software simulation (VCS) and hardware emulation (ZeBu) of the PHY training. The result was a 97x CPU time performance improvement, enabling pre-silicon verification of the entire DDR PHY calibration sequence.

AMS emulation technology can similarly be applied to other AMS designs requiring firmware support, such as filters, converters, SERDES, and power conditioners.

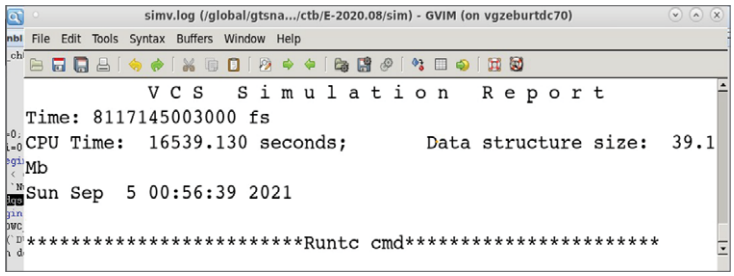


Figure 8: Software training simulation duration

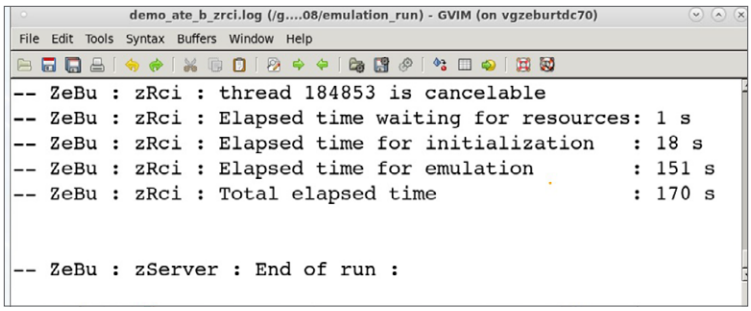


Figure 9: Hardware training simulation duration

## Conclusion

Modern SoCs include a mix of analog and digital components. An increasing number of system peripherals require specialized operations, such as calibration and equalization, to optimize their performance in real-world conditions. These operations are performed by software modules, including drivers and firmware. Verification of the complete system mandates validating that the analog, digital, and software interoperate together. This is difficult or impossible to accomplish since each domain—analog, digital, and software—is typically verified independently using different verification tools. The result is that bugs are found post-silicon and often result in costly chip turns that delay time to market (TTM).

Synopsys AMS Emulation technology resolves this problem by enabling full system validation pre-silicon. This unique solution is possible because the Synopsys ZeBu emulator can concurrently simulate analog, digital, and software system elements in hardware at very high performance. This solution is a game-changer for verification of many types of systems featuring components, such as high-speed memory and interconnect fabrics, filters and converters, and other analog circuits that require digital interfaces tuned under software control. The almost 100x performance boost over software simulation has been validated on commercial designs. Those interested in learning more about AMS Emulation should contact Synopsys.

## About Synopsys

Founded in 1986 in North Carolina, USA, Synopsys is now among the "Top 15" largest software companies in the world and a world leader in the areas of Electronic Design Automation (EDA), Technology Computer Aided Design (TCAD), and Software Quality, Integrity and Security (APPSEC) tools and services. Headquartered in Mountain View, California, Synopsys employs over 16,000 engineering and support staff around the world.

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